Republic of Iraq
The Ministry of Higher Education & Scientific Research

University:Kufa
College:Education for Girls
Department:Computers
Stage:3rd
Lecturer name:Mohammed.H.Dosh
Academic Status:Architecture
Qualification:Computer Msc
Place of work:Najaf

Course Weekly Outline

Course Instructor	Mohammed. H. Ibrahim Dosh				
E_mail	Mohammed.dosh@uokufa.edu.iq				
Title	Computer Architecture				
Course Coordinator					
Course Objective	• **knows all computers components.** • **knows control unit and comparison between its types.** • **manage and allocate memory.** • **Knows the parallel processing.**				
Course Description	Architecture concept: General machine structure, Control unit, Hardwired control, Microprogramming design of CPU control: Instruction format, I/O interfaces, RISC and CISC , Asynchronous data transfer, programmed I/O. Memory management: type and hierarchy, main memory and memory address map, direct memory address ,cache memory. Parallel Processing : pipeline ,arithmetic pipeline , instruction pipeline , interprocessor communication ,cache coherence .				
Textbook					
References	• M.M . Mano "Computer System Architecture" Third Education ,Prntice Hall ,1993 . • David A.Patterson and John L. Hennesy "Computer Organization And Design " Morgan Kaufmann ,1998. • John J. Donovan "Systems Programming" Tata McGraw 1999.				
Course Assessment	Term Tests	Laboratory	Quizzes	Project	Final Exam
	(40%)		(10%)	----	As (50%)
General Notes					

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week	Date	Topics Covered	Lab. Experiment Assignments	Notes
1		Introduction to Computer Architecture and CPU Architecture		
2		Control Unit and overview of Microcontroller		
3		Microprogramming Design of CPU control Unit and Microprogrammed		
4		Instruction Set and Format		
5		RISC and CISC		
6		Program Control (interrupt and subroutine call)		
7		I/O Organization and Peripheral Control Strategies		
8		Input/ Output Interfaces		
9		Asynchronous Data Transfer		
10		Programmed I/O		
11		Hardwired Control		
12		Computer System		
13		Memory management		
14		Type and Hierarchy		
Half-year Break				
15		Main Memory and Memory Address Map		
16		Addressing modes		
17		Direct Memory Access		
18		Input/ Output Processor (IOP)and Channels		
19		Associative Memory and Control –Addressable Memories		
20		Cache Memory		
21		Parallel Processing		
22		Pipeline(general consideration)		
23		Arithmetic Pipeline		
24		Instruction Pipeline		
25		Difficulties in Instruction Pipeline and Theme Solutions		
26		Vector processing and Array Processor		
27		Interprocessor communication		
28		Cache Coherence		

Instructor Signature: **Dean Signature:**